

Claims:

What is claimed is:

- 5 1. A loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

 an integral path circuit that receives an input signal and generates an integrated output signal for tracking an overall input signal level including proportional signals of prior input signals wherein the proportional signals are based on detected
10 instantaneous phase differences for locking a frequency of a signal for a phase locked loop (PLL) circuit to a reference frequency;

 a proportional path circuit coupled in series with the integral path circuit wherein the proportional path circuit receives and differentiates the integral output signal to provide a proportional output signal; and

15 a summer that receives and sums the proportional output signal and the integrated output signal to provide a low-noise loop filter output signal.

2. The loop filter according to Claim 1, wherein the integral path circuit further comprises:

20 an amplifier; and
 an integrating capacitor coupled in parallel with the amplifier.

3. The loop filter according to Claim 1, wherein the proportional path circuit further comprises:

25 a differentiating capacitor;
 a first switch;
 a second switch; and
 a holding capacitor;

wherein the differentiating capacitor and the second switch are coupled in series between the integral path circuit and the summer;

wherein one end of the first switch is coupled between the differentiating capacitor and the second switch and another end of the first switch is coupled to
5 ground; and

wherein one end of the holding capacitor is coupled between the second switch and the summer and another end of the holding capacitor is coupled to ground.

4. The loop filter according to Claim 3, wherein:

10 the first switch is activated and the second switch is deactivated before and during an occurrence of a charge pump output to charge up the differentiating capacitor; and

the first switch is deactivated and the second switch is activated only after the occurrence of the charge pump output to charge up the holding capacitor, which, in
15 effect, filters out noise in the charge pump output.

5. The loop filter according to Claim 4, wherein respective activation and deactivation of the first switch and the second switch are repeated for differentiating various integral output signals to provide corresponding proportional output signals.

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6. The loop filter according to Claim 1, further comprising:

a filter coupled to the low-noise loop filter output signal wherein the filter comprises a resistor and a capacitor coupled in series and between the low-noise loop filter output signal and ground.

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7. The loop filter according to Claim 1, wherein:

the proportional path circuit holds off providing the proportional output signal as an output signal during a noisy period of a phase frequency comparator.

8. A method for implementing a loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

receiving, by an integral path circuit, an input signal and generating, by the
5 integral path circuit, an integrated output signal for tracking an overall input signal level including proportional signals of prior input signals wherein the proportional signals are based on detected instantaneous phase differences for locking a frequency of a signal for a phase locked loop (PLL) circuit to a reference frequency;

receiving and differentiating, by a proportional path circuit coupled in series with
10 the integral path circuit, the integral output signal to provide a proportional output signal; and

receiving and summing, by a summer, the proportional output signal and the integrated output signal to provide a low-noise loop filter output signal.

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9. The method according to Claim 8, further comprising:

coupling an amplifier in parallel with an integrating capacitor to provide the integral path circuit.

20 10. The method according to Claim 8, further comprising:

providing a differentiating capacitor, a first switch, a second switch, and a holding capacitor for the proportional path circuit;

coupling the differentiating capacitor and the second switch in series between the integral path circuit and the summer;

25 coupling one end of the first switch between the differentiating capacitor and the second switch and another end of the first switch to ground; and

coupling one end of the holding capacitor between the second switch and the summer and another end of the holding capacitor to ground.

11. The method according to Claim 10, further comprising:

activating the first switch and deactivating the second switch before and during an occurrence of a charge pump output to charge up the differentiating capacitor; and

5 deactivating the first switch and activating the second switch after the occurrence of the charge pump output to charge up the holding capacitor, which, in effect, filters out noise in the charge pump output.

12. The method according to Claim 11, further comprising:

10 repeating the respective activating and deactivating steps of the first switch and the second switch for differentiating various integral output signals to provide corresponding proportional output signals.

13. The method according to Claim 8, further comprising:

15 further filtering the low-noise loop filter output signal by coupling a resistor and a capacitor in series between the low-noise loop filter output signal and ground.

14. The method according to Claim 8, further comprising:

20 holding off providing by the proportional path circuit the proportional output signal as an output signal during a noisy period of a phase frequency comparator.

15. A method for implementing a loop filter for a phase locked loop ("PLL") circuit which locks a frequency of a signal to a reference frequency, comprising:

25 integrating a loop filter input signal to provide an integrated signal that tracks an overall input signal level;

differentiating the integrated signal to provide a proportional signal based on a detected instantaneous phase difference for locking a frequency of a signal for a phase locked loop (PLL) circuit to a reference frequency; and

summing the integrated signal and the proportional signal to provide a low-noise loop filter output signal.

16. The method according to Claim 15, wherein:

- 5 the integrating step is performed by an integral path circuit;
the differentiating step is performed by a proportional path circuit cascaded to the integral path circuit; and
the summing step is performed by a summer which receives as inputs the integrated signal and the proportional signal.

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17. The method according to Claim 16, further comprising:

coupling the integral path circuit, the proportional path circuit, and the summer in a single cascaded path.

15 18. The method according to Claim 15, wherein the differentiating step further comprises:

differentiating the integrated signal by charging up a differentiating capacitor;
and

20 coupling the differentiating capacitor to a holding capacitor wherein the holding capacitor is charged up only after the occurrence of a charge pump output, which, in effect, filters out noise in the charge pump output, and the holding capacitor holds the charge of the differentiating capacitor as the proportional signal being input into the summer.

25 19. The method according to Claim 15, further comprising:

further filtering the low-noise loop filter output signal by coupling a resistor and a capacitor in series between the low-noise loop filter output signal and ground.

20. The method according to Claim 15, further comprising:
holding off providing the proportional signal as an output signal during a noisy
period of a phase frequency comparator.

5 21. A method of providing a proportional path signal for a loop filter of a phase
locked loop circuit, comprising:

differentiating an integrated signal received from an integral path circuit of a
loop filter of a phase locked loop circuit by utilizing and charging up a differentiating
capacitor according to the integrated signal; and

10 delaying charging up a holding capacitor based on a charge of the
differentiating capacitor until only after an occurrence of a charge pump output of the
loop filter, which, in effect, filters out noise in the charge pump output.